Experimental Digital HF Receiver
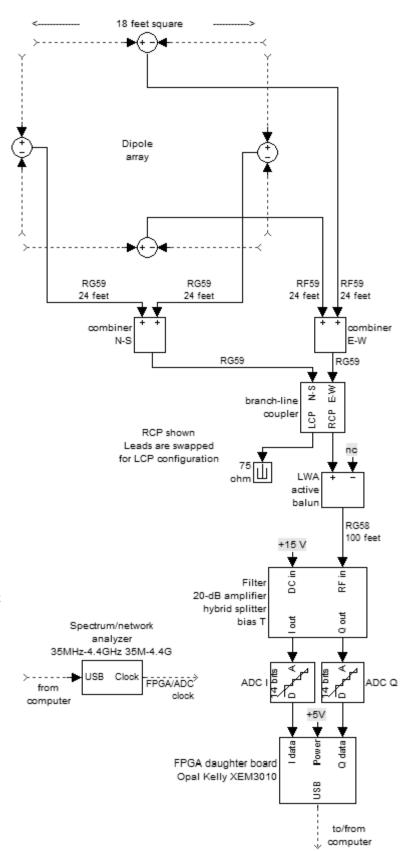
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The receiver consists of an antenna, analog electronics, ADCs, and digital processing in a field-programmable gate array (FPGA).

The antenna consists of four Radio Jove dipoles oriented east/west and north/ south and tuned for about 25 MHz. They are suspended from poles of steel conduit.
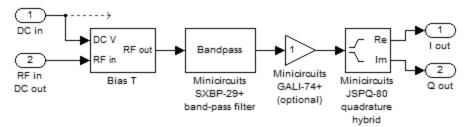
The antenna can be manually switched between circular and linear polarization. In the circular polarization configuration shown in the figure, E/W and N/S pairs are combined by in-phase combiners, which are then combined by a branch-line coupler fashioned from 50- and 75-Ω cable and tuned for a center frequency of 24 MHz. There is active gain in an LWA active balun, which is mounted atop a short PVC pipe and sheltered by plastic. Only one of the two inputs of the active balun is used in this configuration.

In the linear-polarization configuration, the combined pairs are fed in phase to the two inputs of the active balun. This configuration provides sensitivity to linear polarization along one or the other of the two diagonals.

At this point there is no coherent scheme for pointing of the antenna by phasing the segments.
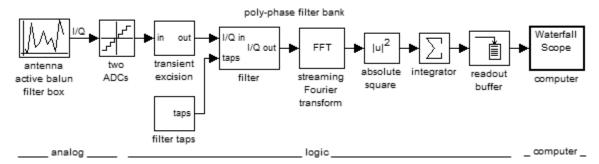
The 'Filter/amplifier/hybrid splitter' box contains a Minicircuits band-pass filter with pass band of roughly 20-40 MHz. The hybrid splitter provides I and Q signals to two ADCs, whose outputs are processed as a single complex data stream.

The ADC board is a borrowed board. Of its eight ADCs, four are still working and two are used. Its ADCs have 14 bits, not all of which are used. The board piggy backs an Opal Kelly XEM-3010 containing a Xilinx Spartan 3 FPGA. This FPGA has sufficient capacity to house the digital processing of a single receiver.

While the logic can upload blocks of the digital data to the computer for conventional FFT processing in software, there is a poly-phase filter bank in logic that is able to process nearly all of the data and deliver spectra to the computer.

The streaming FFT is implemented by the Xilinx core generator. The receiver logic is typically built for 1024 spectral channels. The integration time is programmable, after which the spectrum is transferred to the buffer, integration is deterministically restarted, and the spectrum concurrently uploaded to the computer for recording and display. The receiver is typically clocked at 25.6 MHz so that the spectral resolution is an even 25 kHz.

Because so much processing is done in logic, the computer has only housekeeping functions to perform and very little processing time is needed compared to receiver-in-software. The integration results in reduced movement of data to the computer by orders of magnitude.

Useful bandwidth is about 20 MHz (above 19 MHz) and spot checks of image isolation show typically 30 dB.

While this receiver is sensitive and is capable of good temporal and spectral resolution, its current limitation is that it is easily overloaded by strong spectral lines, limiting the receiver's use during the noisiest times of the day.

There is currently no calibration of the receiver.

References

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- Daniel Zhou, *A review of polyphase filter banks and their application*, http://www.dtic.mil/get-tr-doc/pdf?AD=ADA457390.
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- Xilinx Spartan 3 FPGA, http://www.xilinx.com/products/silicon-devices/fpga/spartan-3.html.
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